

# 1-V Power Supply CMOS Cascode Amplifier

Torsten Lehmann and Marco Cassia

**Abstract**—In this paper, we design a folded cascode operational transconductance amplifier in a standard CMOS process, which has a measured 69-dB dc gain, a 2-MHz bandwidth, and compatible input- and output voltage levels at a 1-V power supply. This is done by a novel current driven bulk (CDB) technique, which reduces the MOST threshold voltage by forcing a constant current through the transistor bulk terminal. We also look at limitations and improvements of this CDB technique.

**Index Terms**—1-V OTA, CMOS, current driven bulk, ultra-low voltage.

## I. INTRODUCTION

ONE OF THE most serious design constraints when making integrated analog circuits for systems with ultra-low supply voltages is the value of the MOS threshold voltage  $V_{th}$ . A typical 3.3-V process has  $V_{th}$  in the range 0.6–0.7 V. Used with a 1-V power supply, this gives a signal swing of at most 100 mV on a transistor gate, if room for two drain–source saturation voltages  $V_{DS,sat}$  of 100 mV is needed (which it most certainly is). Several approaches to ultra-low voltage supply circuit design have recently been described; e.g., based on charge pumps [1], bulk drive [2], floating gates [3] or limited common-mode range input circuits [4], [5]. In this paper, we shall look at how to reduce the MOS threshold voltage in a standard CMOS process, and we shall use the reduced- $V_{th}$  transistors to implement a 1-V folded cascode operational transconductance amplifier (OTA) with compatible input- and output levels. The advantages of this technique are that 1) possible voltage stress, increased power consumption, and noise coupling associated with a charge pump are avoided; 2) the input transistor pair gain reduction and input impedance reduction associated with a bulk drive are avoided; 3) special processing and callibration steps associated with floating gate devices are avoided; 4) continuous time signal processing is possible; and 5) standard circuit topologies, such as cascode amplifiers, can be used. In Section II, we look at the current driven bulk technique for reducing  $V_{th}$ . In Section III, we look at the unwanted effects of this technique and how to overcome these. In Section IV, we implement the OTA. In Section V, we present measurements from an experimental chip, and in Section VI, we draw the conclusions.

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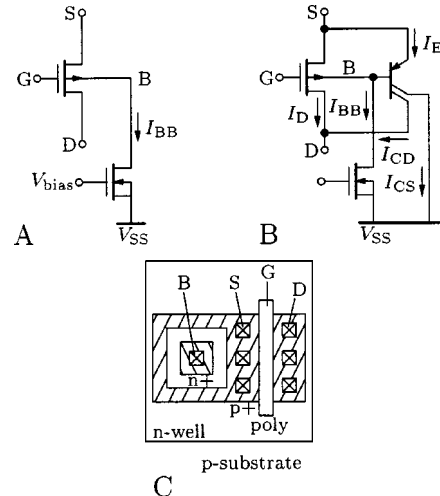


Fig. 1. Current drive of bulk terminal. (a) Circuit. (b) Circuit with parasitic BJT. (c) Layout.

## II. CURRENT DRIVEN BULK

The threshold voltage of a MOS transistor as a function of the bulk–source voltage  $V_{BS}$  is given by

$$V_{th} = V_{th0} + \gamma(\sqrt{|2\phi_F - V_{BS}|} - \sqrt{|2\phi_F|}) \quad (1)$$

where

$V_{th0}$  zero bias threshold voltage;

$\gamma$  bulk effect factor;

$\phi_F$  Fermi potential.

For p-channel transistors,  $2\phi_F \approx -0.7$  V,  $\gamma \approx -0.5\sqrt{V}$ , and  $V_{th0} \approx -0.6$  V, typically, and a bulk bias  $V_{BS}$  is normally  $>0$  V, which numerically increases the threshold voltage. However, by biasing  $V_{BS} < 0$  V we can actually (numerically) decrease the threshold voltage [6], [7].

To reduce the threshold voltage as much as possible, we want the bulk bias  $|V_{BS}|$  as high as possible. This will, however, forward bias the bulk–source diode, i.e., the base–emitter diode of the associated parasitic bipolar transistor (BJT), thereby turning on this BJT; thus,  $|V_{BS}|$  is limited by how much current we can tolerate in the BJT. Now, this is the idea of the new *current driven bulk* (CDB) circuits (see Fig. 1). Instead of voltage driving the bulk where we would need a considerable safety margin to hold the current level in the bipolar transistor below a certain value,  $I_{max}$ , we simply force a current,  $I_{BB} = I_{max}/(\beta_{CS} + \beta_{CD} + 1)$ , through the diode, where the  $\beta$ 's are the two base–collector current gains of the BJT; this will always give us the largest possible bulk bias (namely the diode forward voltage). In Fig. 2 the simulated threshold

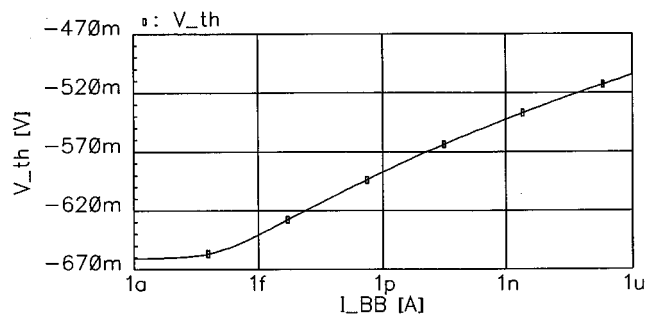


Fig. 2. Threshold voltage versus bulk bias current.

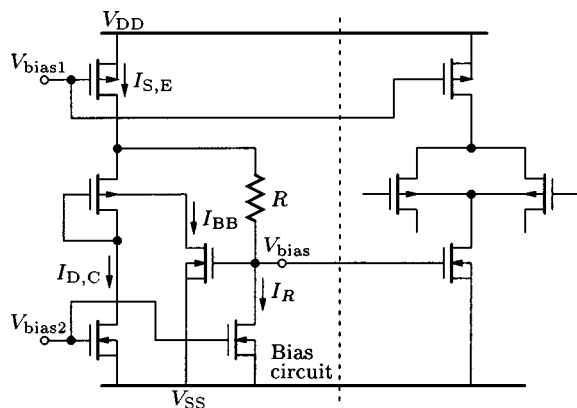


Fig. 3. Bias circuit eliminating unknown BJT  $\beta$ 's.

voltage as a function of the bulk bias current  $I_{BB}$  is shown for a  $W/L = 40 \mu\text{m}/10 \mu\text{m}$  device in a  $0.5\text{-}\mu\text{m}$  process. We use a p-channel transistor as we can access the bulk terminal for this device without fear of latchup in a standard n-well process.

Because of the exponential  $I\text{-}V$  relation of the diode, the exact value of  $I_{BB}$  is not important for the resulting threshold voltage. However, the parasitic bipolar transistor can have quite high base-collector current gains [8]; as we shall see below, this put some limitations on the applicability of the CDB technique. To keep the BJT current gains as low as possible, the layout shown in Fig. 1(c) can be used: to keep the substrate-collector gain ( $\beta_{CS}$ ) low, the bulk connection is completely surrounded by the source junction; to keep the drain-collector gain ( $\beta_{CD}$ ) low, a longer than minimum MOS channel length should be used. In the simulations, we have used current gains in the order of 100.

Another problem with the BJT current gains is that they are usually unknown to the designer. This is solved by “measuring” the current gain using the bias circuit in Fig. 3. A transistor with current driven bulk is set up between a current sink  $I_{D,C} = I_D + I_{CD}$  and a current source  $I_{S,E} = I_D + I_E + I_R$ . The circuit feedback will now cause a bulk bias current  $I_{BB}$ , and hence a bias voltage  $V_{bias}$ , such that  $I_{S,E} = I_D + I_{BB}(1 + \beta_{CS} + \beta_{CD}) + I_R$ , regardless of the actual values of the  $\beta$ 's. For an ideal drain current  $I_D$ , we would probably choose  $I_{D,C} \approx 1.1I_D$ ,  $I_{S,E} \approx 1.3I_D$  and  $I_R \approx 0.1I_D$ . For the bias circuit to work, we must have  $V_{BE} < V_{thN} + I_R R$  and  $|V_{thP}| + V_{DS,sat} < V_{thN} + I_R R$ , where  $V_{thP}$  is the threshold voltage of the current driven bulk device. If the MOST threshold voltages are high compared with

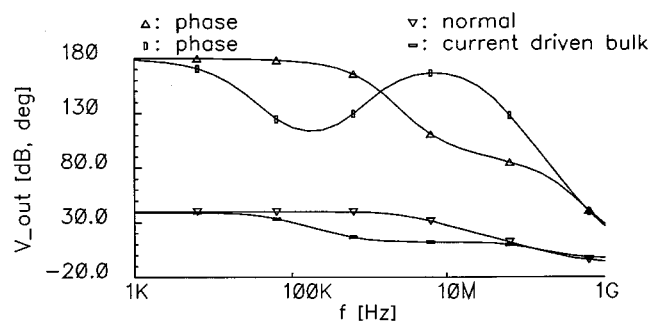


Fig. 4. CDB compared with normal MOST common-source frequency response.

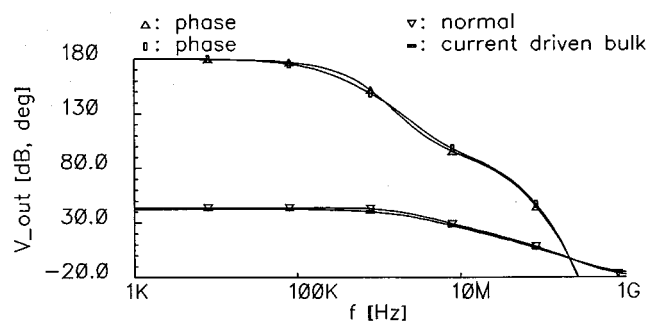


Fig. 5. Cascoded CDB compared with normal MOST common-source frequency response.

a  $V_{BE}$  and if  $|V_{th0P}| \geq V_{th0N}$ , the level shifter  $I_R R$  can be omitted.

### III. CDB UNWANTED EFFECTS

Current driving the bulk introduces a number of unwanted effects in the resulting device. The first obvious one is the parallel connection of the BJT emitter/collector with the MOS source/drain; this must lower the device output impedance. If the BJT emitter current is much smaller than the MOS source current, the effect is negligible. If not, to get a reasonable output impedance, the BJT must be in the active region; i.e., the device drain-source voltage must be less than about  $-200 \text{ mV}$  (simulations can be found in [9]). Noise from the BJT would also enter the circuit, but again, if the current in this device is low, we would expect only a small amount of added noise.

The largest current available for discharging the bulk-drain capacitance is  $I_{BB}$ ; likewise, the largest current available for charging it is the source quiescent current divided by the base-emitter current gain  $I_S/(\beta_{CS} + \beta_{CD} + 1)$ . These are small currents, which means that slew-rate effects might occur if the bulk-drain voltage is changed.

Together with the bulk transconductance and the base-emitter impedance, the drain-bulk capacitance also causes a low frequency pole-zero pair. This can be seen in Fig. 4, which shows the simulated frequency response of a common-source amplifier ( $W/L = 40 \mu\text{m}/1 \mu\text{m}$  device with  $I_{BB} = 30 \text{ nA}$  and  $I_D = 10 \mu\text{A}$ ).

It is evident that the drain-bulk capacitance has a major impact on high-frequency circuit performance. Fortunately, there are several ways to cancel its effect. First, one can put a decoupling capacitor between bulk and source: as both the slew-rate

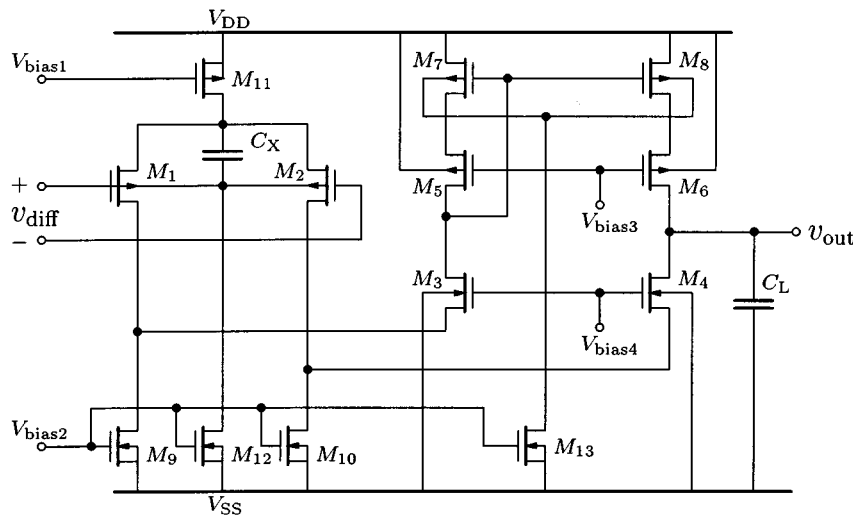


Fig. 6. 1-V CDB folded cascode OTA.

TABLE I  
CDB OTA TRANSISTOR DIMENSIONS

MOST	$W/\mu\text{m}$	$L/\mu\text{m}$	$I_D/\mu\text{A}$	MOST	$W/\mu\text{m}$	$L/\mu\text{m}$	$I_D/\mu\text{A}$
$M_1-M_2$	400	1	10	$M_9-M_{10}$	20	1	20
$M_3-M_4$	20	1	10	$M_{11}$	80	1	20
$M_5-M_6$	40	1	10	$M_{12}$	1	50	$\sim 0.01$
$M_7-M_8$	40	1	10	$M_{13}$	1	50	$\sim 0.01$

and the pole-zero pair are caused by the bulk transconductance through a nonconstant bulk-source voltage, both effects can be canceled this way. If the source is at a constant potential, a cascode can be used to keep the drain potential constant, thus eliminating the current in the capacitor. In Fig. 5, a cascode has been added to the common-source amplifier, and we see how the frequency response is greatly improved. A third way to reduce the slew-rate limitation (for instance in a CDB differential pair) is proposed in [9]: the type II CDB technique. By adding a third collector to the BJT and shorting this to its base, the current available for slewing can be increased by a base-collector current gain.

#### IV. 1-V FOLDED CASCODE OTA

Fig. 6 shows our OTA. It is a standard folded cascode transconductance amplifier with a CDB differential pair, and a CDB output current mirror (for simplicity, a straightforward bias circuit is shown). Assuming a standard strong inversion design with  $V_{DD} = 1$  V,  $V_{SS} = 0$  V,  $|V_{th}| = 0.6$  V, and  $V_{DS,sat} = 0.1$  V, the range of the input common-mode voltage would be

$$\begin{aligned} V_{DS,sat} - |V_{th}| &= -0.5 \text{ V} \lesssim V_{CM} \lesssim 0.2 \text{ V} \\ &= V_{DD} - |V_{th}| - 2V_{DS,sat} \end{aligned} \quad (2)$$

which is not compatible with the output voltage range

$$2V_{DS,sat} = 0.2 \text{ V} \lesssim v_{out} \lesssim 0.8 \text{ V} = V_{DD} - 2V_{DS,sat}. \quad (3)$$

Note that there is only just enough voltage for the cascode current mirror to function, which does not make a particularly good design.

Reducing the threshold voltage of the differential pair ( $M_1-M_2$ ) directly improves the common-mode input range. Also, operating the input pair in subthreshold reduces the gate-source voltage, and improves the common-mode input range. Note that we use only one current source for the common bulk terminal in the pair (rather than individual current drives for each transistor); otherwise, we would have mismatch problems in the pair. Also note that any noise injected because of the current drive will enter the amplifier as a common-mode signal and thus be rejected. Assuming we can reduce the threshold voltage until  $|V'_{th}| = 0.4$  V by current driving the bulk, we now get

$$\begin{aligned} 2V_{DS,sat} - |V'_{th}| &= -0.2 \text{ V} \lesssim V'_{CM} \lesssim 0.6 \text{ V} \\ &= V_{DD} - |V'_{th}| - V_{DS,sat}. \end{aligned} \quad (4)$$

Thus, we now have a 0.4-V overlap in the valid input and output ranges. To get more voltage room for the current mirror, we also current drive the bulk of the transistors in this.

As the drains of all the current driven bulk transistors are cascoded, we will not expect any parasitic poles from the CDB technique. However, when a large common-mode input signal change is applied, the bulk-drain voltage of the input pair will change, which might cause slewing in this stage. We reduce this slewing effect by adding a coupling capacitor  $C_X$  between the bulk and the source of the pair. In such a low-voltage design, it is an advantage to operate the cascoding transistors ( $M_3-M_6$ ) in subthreshold, as that makes it easier to generate the bias voltages  $V_{bias3}$  and  $V_{bias4}$ ; it is, however not critical. The other transistors ( $M_7-M_{13}$ ) should work in strong inversion as good matching gives the lowest overall offset error. The transistor dimensions used in our amplifier are shown in Table I.

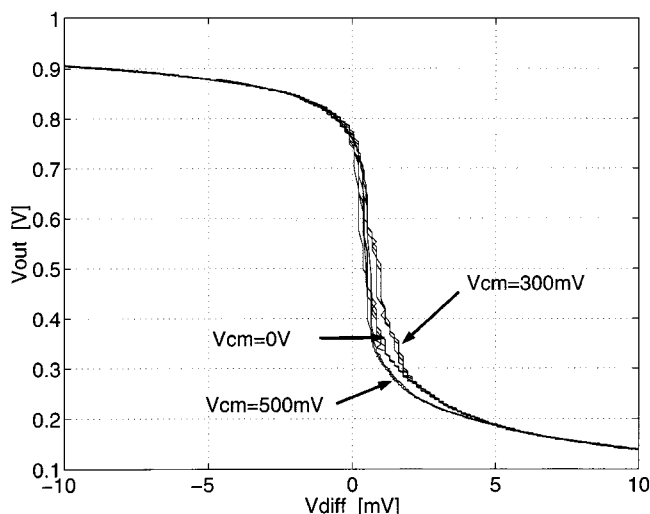


Fig. 7. Measured CDB OTA dc responses at  $V_{DD} = 1.0$  V at different common-mode voltages.

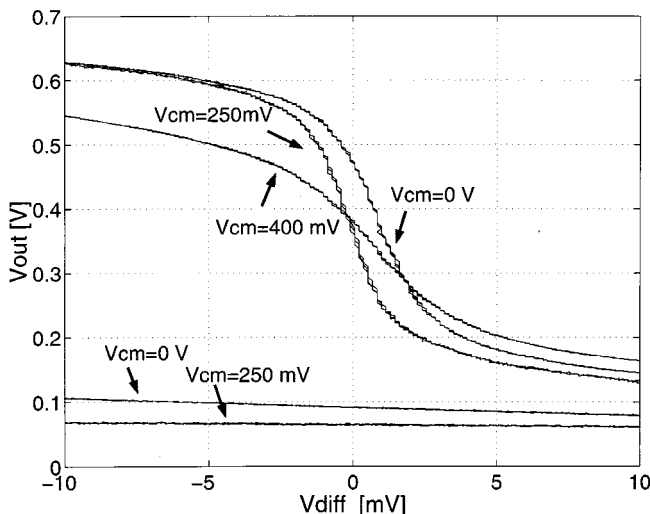


Fig. 8. Measured CDB OTA dc responses at  $V_{DD} = 0.75$  V with and without (two bottom traces) bulk current.

V. MEASUREMENTS

An experimental amplifier has been fabricated in a standard  $0.5\text{-}\mu\text{m}$  CMOS process. It has been designed with a quite high total bias current,  $40\ \mu\text{A}$ , such that it can drive a  $20\text{-pF}$  off-chip capacitive load while having a  $1\text{-MHz}$ -range gain bandwidth (a version for on-chip applications is straightforward to do by transistor scaling). The coupling capacitor  $C_X$  can be chosen to  $10$  or  $0$  pF. The nominal value of the bulk current is  $I_{BB} = 10$  nA, which (given a BJT current gain of about  $100$ ) gives a  $10\%$  increase in the differential pair quiescent current. The strong inversion transistors have been designed to operate with effective gate-source voltages around  $100$  mV.

Fig. 7 shows the measured dc transfer function of our amplifier for different common-mode input voltages, using a  $1\text{-V}$  power supply; the high-gain region is readily identified. We also notice that the input referred offset error of the amplifier is less than  $1$  mV. Fig. 8 shows the dc transfer function using a  $0.75\text{-V}$  power supply; this figure also show the transfer function when

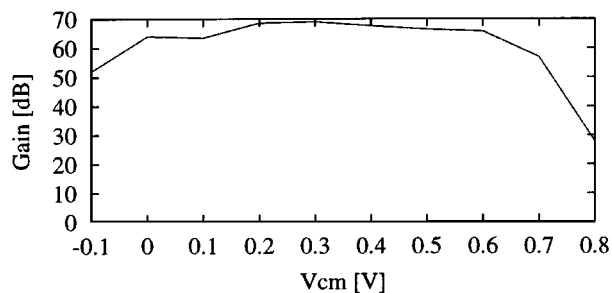


Fig. 9. Measured CDB OTA dc gain at  $V_{DD} = 1.0$  V.

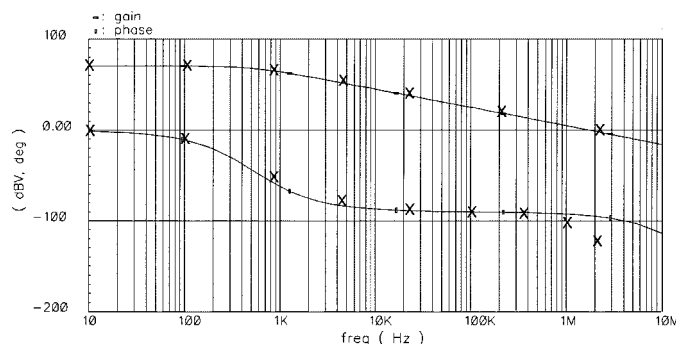


Fig. 10. Measured ( $X$ ) and Simulated ( $—$ ) CDB OTA ac responses.

no transistors are driven with a bulk current. It is evident that our CDB technique enables us to use this ultra-low power supply.

Fig. 9 shows the dc gain as a function of the common-mode input voltage. We see that at a  $1\text{-V}$  power supply, we have a  $0.65\text{-V}$  common-mode input range in which the amplifier has at least a  $62\text{-dB}$  gain; and an overlap of about  $0.3$  V in the input and output voltage ranges. Fig. 10 compares the measured and simulated ac characteristics of the amplifier when loaded with  $20$  pF. The measured and simulated amplitude characteristics agree very well. The measured phase margin is somewhat worse than the simulated one. This is probably due to inaccurate modeling of the BJT. Quantitatively, the measurements are the same for all common-mode input voltages; also, they are the same regardless of whether  $C_X$  is present or not. The slew rate is also virtually independent of the presence of  $C_X$ , and the CDB-induced slewing shows only at a  $0.7\text{-V}$  power supply, which could be because the BJT current gain is low. It has a gain bandwidth of  $2$  MHz and a phase margin of  $57^\circ$ . These are all respectable data for any  $1\text{-V}$  amplifier, which means that the CDB technique can be applied wherever low-voltage LF analog signal processing is required (e.g., in hearing aids, implants, watches, or similar battery operated devices). Table II summarizes the amplifier characteristics.

VI. CONCLUSION

In this paper, we implemented an ultra-low supply voltage folded cascode OTA in a standard CMOS process. At a  $1\text{-V}$  power supply, it has a  $0.3\text{-V}$  overlap in the allowed input common-mode range and the output voltage range, a dc gain of  $69$  dB and a  $2\text{-MHz}$  bandwidth. The amplifier works with a power supply of less than  $0.8$  V (with a somewhat degraded performance, though). This design was made possible by a new technique to lower the MOST threshold voltage, current driven

TABLE II  
CDB OTA MEASURED FIGURES OF MERIT

Supply voltage	1.0 V	0.8 V	0.7 V
Common-mode input range	0.0 V–0.65 V	0.0 V–0.4 V	0.0 V–0.3 V
High gain output range	0.35 V–0.75 V	0.25 V–0.5 V	0.2 V–0.4 V
Output saturation limits	0.1 V–0.9 V	0.15 V–0.65 V	0.1 V–0.6 V
DC gain	62 dB–69 dB	46 dB–53 dB	33 dB–36 dB
Gain-bandwidth	2.0 MHz	0.8 MHz	1.3 MHz
Slew-rate	0.5 V/ $\mu$ s	0.4 V/ $\mu$ s	0.1 V/ $\mu$ s
Phase margin	57°	54°	48°

bulk, where we force a constant current out of the bulk terminal. Initially, the drain–bulk capacitance gives these circuits poor high-frequency performance, but its effect can be compensated for using cascodes as experimentally verified—or by using additional circuits in the CDB structure.

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